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Silicon bulk issues during processing of homo-heterojunction solar cells

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Abstract

In this work, an emerging cell concept based on silicon homo-heterojunction (HHJ) is investigated. Compared to the n-type silicon heterojunction cell (HET), the HHJ architecture contains an additional thin and highly doped (p^+)c-Si layer at the front (i)a-Si:H/(n)c-Si interface. Using numerical simulations, advantages of the alternative architecture are first underlined. Especially, passivation improvements brought by the (p^+)c-Si layer are evidenced through the study of the recombination rates in the whole cell. From the simulation results, the manufacturing issues of the HHJ cell are then addressed. Due to the need of a fully activated and shallow (p^+)c-Si layer, ion implantation of boron is a promising candidate for making such cells. However, the efficient (i)a-Si:H passivation is very sensitive to substrate quality. Thus, the high temperature post-implantation annealing effect on the Cz substrates should to be assessed. An anneal at 1050°C, often required to fully activate Boron implanted emitters, strongly decreases the substrate lifetime and will impact drastically the HHJ cell performance. A 950°C annealing is found to limit considerably the substrate degradation. However, such rather low temperature will limit the maximum doping concentration of the implanted layer and thus the maximum achievable V_{OC} in HHJ devices.

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Keywords: silicon heterojunction, simulation, homo-heterojunction, hetero-homojunction, emitter, ion implantation, activation annealing, Boron ;

1. Introduction

Amorphous/crystalline silicon heterojunction is a very promising photovoltaic cell technology thanks to its potential to achieve high power conversion efficiency at relatively low manufacturing cost [1]. In today's

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heterojunction (HET) cells, the c-Si surface passivation is identified as a key issue to reach high efficiency and it is especially critical for the p/n junction [2,3]. Therefore, ways to further improve the (p)a-Si:H/(i)a-Si:H/(n)c-Si contact quality should be investigated to enhance cells performance. On the one hand, the density of interface recombination centers (D_{it}) can be reduced by surface cleaning or by improving the (i/p)a-Si:H stack passivation capability [3]. On the other hand, a higher band bending can decrease interface recombination [4], leading to more efficient devices. The latter route could be realized through the addition of a thin and highly doped (p^+)c-Si layer underneath the (i)a-Si:H passivation layer [1], thus enhancing the field effect passivation. The resulting structure, introduced in Figure 1, is called a homo-heterojunction (HHJ).

In this work, the key aspects of the HHJ cell, inferred from numerical simulations, are first introduced with a particular emphasis on recombination processes at interfaces and in the substrate. The new architecture is compared to the HET cell and its advantages are underlined. Then, a focus is made on the optimization of the added (p^+)c-Si layer in order to maximize the HHJ cell efficiency regarding the manufacturing process.

Experimentally, the effect of boron-implanted dopant activation upon annealing on the c-Si substrate is evidenced. Because open circuit voltages above 720 mV are targeted, substrate degradation upon annealing is critical when using high quality surface passivation. The effect on Cz n-type c-Si substrates of annealing at 950°C and 1050°C is investigated and discussed regarding the homo-emitter manufacturing for the HHJ technology. Finally, rapid thermal annealing is tested as a way to reduce considerably the process thermal budget.

2. Homo-heterojunction cell simulation

The main features of the homo-heterojunction (HHJ) cell recently studied by numerical simulation by our team are worth to be recalled [5]. The simulation relies on an n-type heterojunction (HET) cell model fitting our state-of-the-art INES cell. From this cell, a thin (10 nm) and highly doped ($N_A = 5\times10^{18}$ cm^{-3}) (p^+)c-Si layer is added at the c-Si/a-Si:H front interface on the emitter side. The emitter lifetime was set slightly lower than real diffused emitters in order not to overestimate the potential benefit of inserting this (p^+)c-Si layer. HET and HHJ cell performances versus the front interface states density, D_{it}, are plotted Figure 2, (capture cross sections for both types of carriers were set to 3×10^{-15} cm^2)

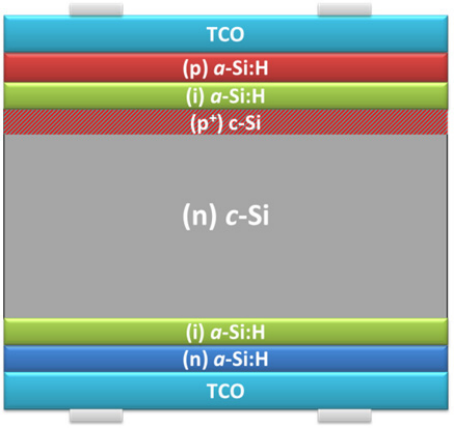

Figure 1: Scheme of the HHJ cell with its the added (p^+)c-Si layer

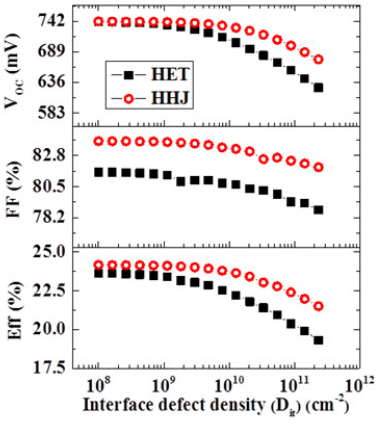

Figure 2: HET (■) and HHJ (○) cells output parameters versus D_{it}.

Compared to the HET reference, the HHJ cell displays V_{OC} and FF improvements leading to significantly higher conversion efficiency. Moreover, the HHJ cell has a reduced D_{it} sensitivity. Therefore, the HHJ cell is a promising solution for improving the HET cell efficiency.

V_{OC} and FF improvements have been explained by simulation by electrons repulsion from the limiting hetero-interface, i.e. from field effect passivation. Since recombinations at the interface become more critical at high D_{it},

the interface improvement explains the lower V_{OC} dependence of the HHJ cell upon D_{it}. As a result, for a given D_{it}, recombinations are found to decrease at the interface and to slightly increase in the substrate (see Figure 3). Integrated recombination rates over the layer thickness evidence the substrate as limiting the HHJ cell performance (whereas the HET cell has the higher integrated recombination rate at the front interface). Therefore, in the HHJ architecture, the substrate quality has a larger importance.

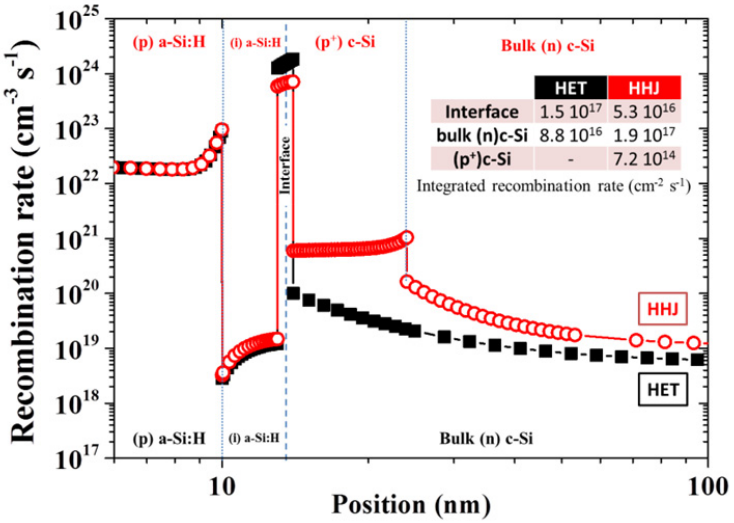

Figure 3: Recombination rate in the HET (■) and HHJ (○) cells in V_{OC} conditions.

It is worth to mention that the simulation study clearly underlines the capability of the HHJ structure to overcome the HET cell limitation. However, the (p^+)c-Si region has been simulated as a uniformly doped layer without modifying the other properties of the reference HET cell. Therefore, the experimental achievement of such an added layer is one of the challenges for a successful device realization.

3. Maximizing the added layer benefits: annealing temperature requirements

As shown in [5], to maximize the HHJ efficiency, the (p^+)c-Si layer should be shallow, with a high doping level and a very low defect density. Therefore, ion implantation which is capable of manufacturing very shallow and well activated junctions is a promising process to obtain adapted junctions.

Implanted cells precursor with contactable boron emitters (i.e. thick emitters) and passivation layers with i-V_{OC} approaching 700mV have already been achieved [6]. They demonstrate the potential of ion implantation to process high quality emitters. Shallow junctions can be performed using low energy beam-line ion implantation or plasma immersion ion implantation. Since the implantation energy should be low in any case, the boron dose and the activation annealing are the two parameters to investigate to succeed in the HHJ realization.

In order to increase the layer doping, the boron dose has to be increased. Moreover, to minimize the recombination, the implanted atoms should be well electrically activated and the concentration of implantation defects should be limited. Both requirements are performed thanks to strong activation annealing, i.e. high annealing temperature for sufficient time [7]. A 950°C anneal is likely to activate low boron dose (10^{14} cm^{-2}) whereas a 1050°C anneal is required for larger doses (10^{15} cm^{-2}) [8,9].

The use of such high annealing temperatures might not be without consequences for the substrate lifetime: detrimental phenomena such as metallic contamination or oxygen precipitation are likely to occur [10] and to decrease the substrate lifetime. Additionally, the high quality of the a-Si:H passivation used in the HET technology will be sensitive to slight substrate degradations. Therefore, a first step toward the experimental achievement of the HHJ cell is to investigate the post-implantation annealing on the Cz silicon bulk in regard to this application.

4. Effect of annealing on substrate properties

4.1. Experiment

160 to 180 µm thick n-type textured Cz 156 cm^2 substrates of 5 different suppliers with resistivities ranging from 2.0 to 6.1 Ω cm are thermally annealed at 950°C or 1050°C in N_2 for 5 min. For Supplier4, substrates from both the top and the bottom of the Cz ingot are tested. For 950°C annealed samples, the initial interstitial oxygen and thermal donors (TD) concentrations are quantified on a twin substrate using the OxyMap technique [11]. The sample surfaces are passivated by a 31 nm thick (i)a-Si:H layer and the lifetime is measured by a WCT-120 Sinton Instrument setup. Then, in order to discriminate surface from bulk changes, for 1050°C annealed samples, 20 µm of their surface have been etched before being passivated again.

4.2. Results and discussions

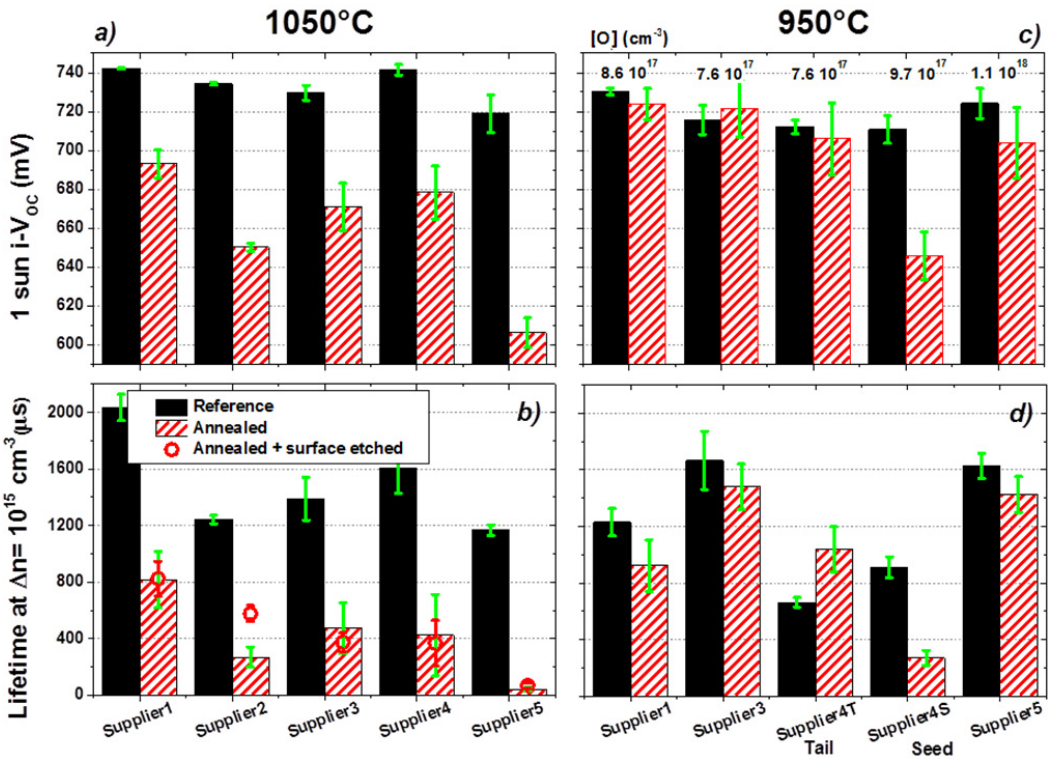

Figure 4: 950°C and 1050°C annealing effect on various Cz substrates passivated with 31 nm thick a-Si:H. The lifetime of the 1050°C annealed substrates is also measured after a chemical etch of the first 20 µm of silicon in order to discriminate surface and bulk losses (○). Error bars represent the standard deviations of measurements performed on four samples.

From Figure 4.a it is seen that all samples lose 40 to 140 mV of implied V_{OC} upon a 1050°C annealing. Therefore, independently of the supplier, such annealing is highly detrimental to Cz c-Si substrates and it is absolutely not suitable for high efficiency HHJ cells realization. Because of the intrinsic a-Si:H passivation (i.e. with little field effect), the effective lifetime at an excess carrier density $\Delta n = 10^{15}$ cm^{-3} gives a better insight of the substrate quality (see Figure 4.b). After the surface etch (red circles) the substrate lifetime of annealed samples is not changed (except for Supplier2 samples), meaning that the degradation occurs in the whole substrate rather than at the surface.

From Figure 4.c, the 950°C annealing is found to have a reduced impact on the substrates, especially for substrates displaying limited oxygen content ($[O_i] < 9\times10^{17}$ cm^{-3}). Then, oxygen precipitation is likely to be the predominant degradation phenomenon. Even if a 950°C annealing is not likely to fully activate a high boron dose, it seems nevertheless adapted for substrates with limited oxygen content. However, from Figure 4.d, a lifetime decrease at low injection level is observed for some substrates evidencing that the annealing was not harmless to the substrates. Consequently, the HHJ cell performance under low illumination regimes (< 1 sun) could be actually decreased. Surprisingly, Supplier4 tail's substrates have their lifetime increased upon thermal annealing. TD annealing could have been an explanation to such a lifetime increase upon annealing [12] but these substrates display a very low initial TD concentration ($1.0\pm0.3\times10^{14}$ cm^{-3}).

This experiment has shown that the post-implantation annealing is a key parameter for achieving a high performance HHJ cell without damaging the c-Si substrate. A 1050°C annealing under N_2 atmosphere may strongly damage the substrate and therefore cannot be used for the homo-emitter activation in the case of an a-Si:H passivation. A 950°C annealing displays a reduced impact on the Cz wafers and might be suitable for boron activation. However, such temperature also restricts the maximum (p^+)c-Si layer doping to low implantation dose (10^{14} cm^{-3}) [8].

4.3. Alternative solutions

Rapid thermal annealing (RTA) which displays very sharp heating and cooling ramps appears as a very interesting candidate to reduce the thermal budget during the activation annealing. However, its limited activation capability has been underlined [7,13]. The implied V_{OC} of samples annealed using RTA are introduced Figure 5. For this experiment, double side polished wafers from a sixth supplier were used.

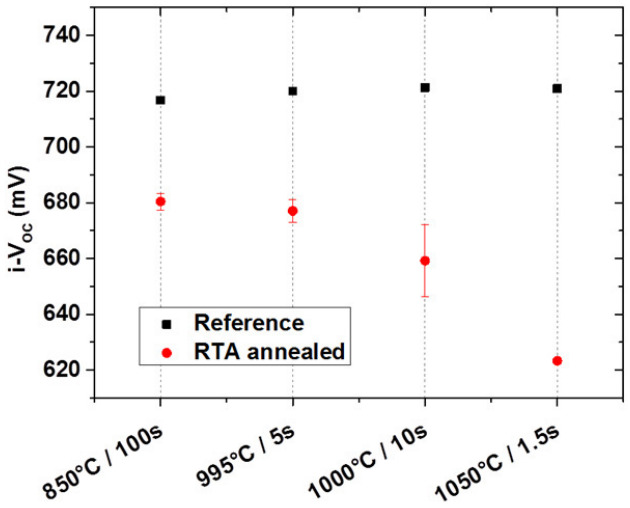

Figure 5: Rapid thermal annealing effect on implied V_{OC}

Despite the very short annealing time, the substrate degradation is found even stronger with the 850°C RTA (-40 mV and 650µs at $\Delta n = 10^{15}$ cm^{-3}) than for the 950°C thermally annealed samples. For RTA annealed samples, due to the very short processing times, the passivation loss seems not to be caused by oxygen precipitation [14]. Additionally, there is a clear correlation between the annealing temperature and the implied V_{OC} loss, independently of the annealing time. In any case, in the present form, the RTA process is not suitable for achieving efficiently activated boron emitters without damaging the silicon bulk. Further work is under way to identify the origin of the observed degradation, in particular with regards to metal contaminants.

Finally, it has been shown recently that epitaxy allows one to grow ultra-shallow layers (<100 nm) with very low recombination current density, i.e. high quality emitters, at temperature lower than 900°C [15]. Thus it also appears as a promising alternative way to achieve the (p^+)c-Si emitter in a HHJ cell.

5. Conclusion

The homo-heterojunction architecture is a very promising solution to enhance the performance of the standard heterojunction solar cell. In order to benefit from the new cell architecture, the implanted additional (p^+)c-Si layer requires a high temperature treatment to properly activate the boron atoms and limit the remaining implantation defects. However, we have shown that a 1050°C annealing for 5 min is very detrimental to the bulk lifetime and thus will limit the V_{OC} of the solar cell even with the excellent a-Si:H passivation. We have evidenced the need of low activation temperature anneal (950°C) and thus the requirement of targeting low boron dose (10^{14} cm^{-3}) for the (p^+)c-Si layer. However, the origin of the observed substrate degradation should be further investigated in order to adapt the annealing process to the targeted application. More precisely, it seems important to dissociate intrinsic silicon substrate loss phenomena (oxygen precipitation, vacancy related effects, etc) from the annealing process chamber environment (e.g. metal contamination).

Acknowledgements

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